BT-3/D-20 43133

DIGITAL ELECTRONICS
ES-207-A/ES-205A

[Time: Three Hours] [Maximum Marks : 75]

Note : All questions in Part A and Part B are compulsory.
Attempt any four from Part C, selecting one question
from each Unit.

Part-A

1. Answer the following question: **15**

   i) Explain the working of NAD operation using NOR gate.

   ii) What is BCD code? What are its advantages and disadvantages? Express the following numbers into BCD 874, 347.

   iii) Explain designing and working of half subtractor.

   iv) State the difference between positive edge triggering of flip-flops.

   v) Write down the specifications of D/A converters.

Part-B

2. Write the significance of gray code. Design a 4 bit gray to binary converter. Express 27 in gray code. **5**
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UNIT–II

3. What is a demultiplexer? Explain the working of l:n demultiplexer using logic diagram. **5**

4. Differentiate between a flip-flop and a Latch. Explain the working of J-K flip-flop. Also explain the problem associated with J-K flip-flop. **5**

5. Draw the basic circuit of a Rom cell. Explain its working.

Part-C

UNIT- I

6. Explain the steps of minimization in Q-M method. Using Q-M method, obtain the minimal expression for F=$\sum$m (6, 7, 8, 9, 13, 15)+d (10, 11, 12, 14). Also realize the expression using NAND gate only. **10**

7. a) Write in detail the characteristics of digital logic gates. Explain them.
   b) Explain the working of CMOS NAND gate. **10**

UNIT-II

8. a) State and explain the working of BCD adder with its logic diagram. **6**

   b) What is encoder? Design a 8;3 encoder. **4**

9. What do you mean by multiplexer? Explain the working of n;l

mux. Design a multiplexer tree for 32:1 mux using 8:1 and 2:1 mux. **10**

UNIT-III

10. a) Design a mod 10 asynchronous counter.

   b) Design a synchronous mod-6 counter. Use JK flip-flop for designing the counter. **10**

11. a) What do you mean by register? Draw and explain the logic diagram of serial in serial out shift right register.

   b) Explain, how SR flip-flop can be converted into JK flip-flop. **10**

UNIT-IV

12. What are the different types of memories? Explain them. **10**

13. What do you mean by PLD? Discuss different types of PLD. Implement the following Boolean functions using PLA:

   $f_1(A, B, C)=\sum m(1, 2, 4, 6)$, $f_2(A, B, C)=\sum m(0, 1, 5, 7)$, $f_2(A, B, C)=\sum m(1, 2, 3, 5, 7)$. **10**

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